## ABSTRACT

A method is described for forming three or more spacer widths in transistor regions on a substrate. In one embodiment, different silicon nitride thicknesses are formed above gate electrodes followed by nitride etching to form spacers. Optionally, different gate electrode thicknesses may be fabricated and a conformal oxide layer is deposited which is subsequently etched to form different oxide spacer widths. A third embodiment involves a combination of different gate electrode thickness and different nitride thicknesses. A fourth embodiment involves selectively thinning an oxide layer over certain gate electrodes before etching to form spacers. Therefore, spacer widths can be independently optimized for different transistor regions on a substrate to enable better drive current in transistors with narrow spacers and improved SCE control in neighboring transistors with wider spacers. Better drive current is also obtained in transistors with shorter polysilicon thickness.